

INFORMATION DISCLOSURE CITATION

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		U.S. PATENT	DOCUMENTS		,	
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	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
LT, N-E,	Higashi, K. et al., "A Manufacturable Copper/Low-k SiOC/SiCN Process Technology for 90nm-node High Performance eDRAM", Proceeding of the IEEE2002 International Interconnect Technology Conference, pp. 15-17, (June 2002).
LT N-E	Fayolle, M. et al., "Intergration of Cu/SiOC in Dual Damascene interconnect for 0.1μm technology using a new SiC material as dielectric barrier", Proceeding of the IEEE2002 International Interconnect Technology Conference, pp. 39-41, (June 2002).
L.T. N-E.	Kim, T.S. et al., "Intergration of Organosilicate Glasses (OSGs) In High Performance Copper Interconnects", Advanced Metallization Conference 2001, pp. 25-31, (October 2001)
L.J. N-E	Fayolle, M. et al., "Overcoming resist poisoning issue during Si-O-C dielectric integration in Cu Dual Damascene interconnect for 0.1 µm technology", pp. 509-513, (October 2001).
L.T.M-E	Lin, J.C. et al., "Via First Dual Damascene Integration of nanoporous Ultra Low-k Material", IEEE2002 International Interconnect Technology Conference, pp. 48-50, (June 2002).

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